

1 LOW-POWER CONTENT ADDRESSABLE MEMORY CELL

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5 BACKGROUND OF THE INVENTION

6 Field of the Invention

7 The present invention relates to content addressable
8 memory (CAM) cells. More specifically, the present
9 invention relates to nine transistor CAM cells and methods
10 for operating these cells in an array.

11
12 Discussion of Related Art

13 CAM cells are defined as memory cells that are
14 addressed in response to their content, rather than by a
15 physical address within an array. Fig. 1 is a block
16 diagram of a conventional memory array formed using twelve
17 CAM cells. The CAM cells are labeled $M_{x,y}$, where X is the
18 row of the array, and Y is the column of the array. Thus,
19 the array includes CAM cells $M_{0,0}$ to $M_{2,3}$. Each of the CAM
20 cells is programmed to store a data value. In the
21 described example, the data value stored in each CAM cell
22 is indicated by either a "0" or a "1" in brackets. For
23 example, CAM cells $M_{0,0}$, $M_{0,1}$, $M_{0,2}$ and $M_{0,3}$ store data values
24 of 0, 1, 0 and 0, respectively. Each row of CAM cells is
25 coupled to a common match line. For example, CAM cells
26 $M_{0,0}$, $M_{0,1}$, $M_{0,2}$ and $M_{0,3}$ are coupled to match line $MATCH_0$.

27 The array of CAM cells is addressed by providing a
28 data value to each column of CAM cells. Thus data values
29 D_0 , D_1 , D_2 and D_3 are provided to columns 0, 1, 2 and 3,
30 respectively. Note that complementary data values $D_0\#$,
31 $D_1\#$, $D_2\#$ and $D_3\#$ are also provided to columns 0, 1, 2 and
32 3, respectively. If the data values stored in a row of

the CAM cells match the applied data values D_0 - D_3 , then a match condition occurs. For example, if the data values D_0 , D_1 , D_2 and D_3 are 0, 1, 0 and 0, respectively, then the data values stored in the CAM cells of row 0 match the applied data values. Under these conditions, the $MATCH_0$ signal is asserted high. Because the applied data values D_0 , D_1 , D_2 and D_3 do not match the data values store in the CAM cells of rows 1 or 2, the $MATCH_1$ and $MATCH_2$ signals are de-asserted low. The match signals $MATCH_0$ - $MATCH_2$ can be used for various purposes, such as implementing virtual addressing, in a manner known to those skilled in the art.

Many different types of CAM cells have been designed. Important considerations in the design of a CAM cell include: the number of transistors required to implement the cell, the power required to operate the CAM cell, and the speed of the CAM cell. In general, it is desirable to have a CAM cell that is implemented using a relatively small number of transistors, such that the layout area of the CAM cell is minimized. It is also desirable for the CAM cell to have a low power requirement and a fast operating speed.

Fig. 2 is a circuit diagram of a conventional nine transistor (9-T) CAM cell 10. CAM cell 10 is described in detail in U.S. Patent No. 4,723,224. CAM cell 10 includes a conventional static random access memory (SRAM) cell 12 and an exclusive OR (XOR) gate 14. SRAM cell 12 includes access transistors 20 and 22, and cross-coupled inverters 16 and 18. Access transistors 20 and 22 are coupled to word line 28 and bit lines 24 and 26, as illustrated. Driver circuitry 36 provides a data value (D) and the inverse of the data value ($D\#$) to bit lines 24 and 26, respectively, during write and compare operations.

SRAM cell 12 is written like a conventional SRAM cell. That is, a logic high value is applied to word line 28, and data values D and D# are applied to bit lines 24 and 26, respectively. As a result, the data values D and D# are latched by inverters 16 and 18, such that the data value D is provided at the output of inverter 18, and the inverted data value D# is provided at the output of inverter 16.

XOR gate 14 includes n-channel transistors 30 and 32, which are connected in series between bit lines 24 and 26. The output terminal of inverter 16 is connected to the gate of transistor 30, such that the inverted data value D# stored in SRAM cell 12 is provided to the gate of transistor 30. Similarly, the output terminal of inverter 18 is connected to the gate of transistor 32, such that the data value D stored in SRAM cell 12 is provided to the gate of transistor 30. Transistors 30 and 32 are commonly connected at node 34, which forms the output terminal of XOR gate 14. Node 34 is connected to the gate of n-channel transistor 38. Transistor 38 has a source coupled to ground line 42, and a drain coupled to match line 40.

CAM cell 10 performs a compare operation as follows. Driver circuitry 36 applies a comparison data value (C) and its complement (C#) to bit lines 24 and 26, respectively. If the comparison data value C matches the data value D stored in SRAM cell 12, then node 34 is connected to receive a logic "0" signal. As a result, transistor 38 is turned off, thereby isolating match line 40 from ground line 42. Under these conditions, match line 40 retains a pre-charged logic high value.

Conversely, if the comparison data value C does not match the data value D stored in SRAM cell 12, then node

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34 is connected to receive a logic "1" signal. As a result, transistor 38 is turned on, thereby coupling match line 40 to ground line 42. Under these conditions, match line 40 is pulled down toward ground.

CAM cell 10 exhibits relatively high power consumption because the same driver circuitry 36 is used to supply the write data values as well as the comparison data values. Driver circuitry 36 is powered by the V_{CC} supply voltage, such that both the write and comparison data values have logic high values of V_{CC} . Moreover, the compare operation of CAM cell 10 is relatively slow because the capacitance of SRAM cell 12 is coupled to bit lines 24 and 26 during the compare operation.

It would therefore be desirable to have an improved CAM cell which allows a compare operation to be carried out using a supply voltage less than the V_{CC} supply voltage. It would also be desirable for the improved CAM cell to have bit lines that are not coupled to the capacitance introduced by an SRAM cell during a compare operation. It would also be desirable for the improved CAM cell to be implemented using fewer transistors than conventional CAM cell 10. It would further be desirable for the improved CAM cell to have global and local masking capabilities.

SUMMARY

Accordingly, the present invention provides a CAM cell that implements a match line having a signal swing equal to one transistor threshold voltage, or about 0.3 Volts. The operating power of the CAM cell of the present invention is relatively low because the match line only

undergoes a small voltage swing during a compare operation.

A CAM in accordance with the present invention includes an SRAM cell that operates in response to a V_{CC} supply voltage. One or more read/write bit lines are coupled to the SRAM cell, thereby allowing read and write data values to be transferred to and from the SRAM cell. The V_{CC} and ground voltage supplies provide signals to the read/write bit lines. That is, the signals applied to the read/write bit lines vary between a high voltage of V_{CC} and a low voltage of 0 Volts.

One or more comparison bit lines are coupled to receive a comparison data value. The signals transmitted on the comparison bit lines have a signal swing that is less than the V_{CC} supply voltage. In one embodiment, the signal swing on the comparison bit lines is equal to two times the transistor threshold voltage. Thus, if the transistor threshold voltage is equal to 0.3 Volts, then the signal swing on the comparison bit lines is equal to 0.6 Volts. Because the comparison bit lines are not directly connected to the SRAM cell, the capacitance of the SRAM cell is advantageously not coupled to the comparison bit lines. This improves both operating speed and power consumption of the CAM cell.

Moreover, the signals transmitted on the comparison bit lines are generated by a bit line control circuit that is powered in response to a supply voltage V_{CC1} that is significantly lower than the V_{CC} supply voltage. In one embodiment, the supply voltage V_{CC1} can have a value as low as 0.9 Volts. By lowering the supply voltage required to perform a compare operation, the power of operating the CAM is advantageously reduced.

1 A sensor circuit is provided for comparing the data
2 value stored in the CAM cell with the comparison data
3 value provided on the comparison bit lines. The sensor
4 circuit pre-charges the match line prior to a compare
5 operation. If the data value stored in the CAM cell does
6 not match the comparison data value, the match line is
7 pulled down. The signal swing of the match line is
8 smaller than the V_{CC} supply voltage. In one embodiment,
9 the signal swing on the match line is equal to transistor
10 threshold voltage, or 0.3 Volts.

11 The sensor circuit monitors the voltage on the match
12 line to determine whether the comparison data value
13 matches the data value stored in the CAM cell (a match
14 condition), or whether the comparison data value fails to
15 match the data value stored in the CAM cell (a no-match
16 condition). The sensor circuit converts the small swing
17 signal on the match line to a large swing output signal.
18 This output signal has a signal swing equal to the V_{CC}
19 supply voltage.

20 In one embodiment of the invention, a bit line
21 control circuit is provided to control the voltages on the
22 comparison bit lines. The bit line control circuit
23 equalizes the voltages on the comparison bit lines to an
24 intermediate voltage prior to each compare operation. As
25 a result, less power is consumed during the compare
26 operation. In one embodiment the intermediate voltage is
27 equal to a transistor threshold voltage (e.g., 0.3 Volts).

28 The present invention will be more fully understood
29 in view of the following description and drawings.
30

1 BRIEF DESCRIPTION OF THE DRAWINGS

2 Fig. 1 is a block diagram of a conventional array of
3 CAM cells;

4 Fig. 2 is a circuit diagram of a conventional nine
5 transistor CAM cell;

6 Fig. 3, which consists of Figs. 3A and 3B as
7 illustrated, is a schematic diagram of a 2x2 array of
8 nine-transistor CAM cells in accordance with one
9 embodiment of the present invention;

10 Figs. 4A and 4B are schematic diagrams of diode
11 connected transistors that can be used in various
12 embodiments of the invention;

13 Fig. 4C is a schematic diagram of a diode-connected
14 transistor and a local masking transistor in accordance
15 with another embodiment of the invention;

16 Fig. 5 is a schematic diagram of the sensor circuit
17 of Fig. 3 in accordance with one embodiment of the present
18 invention;

19 Fig. 6 is a schematic diagram of the bit line control
20 circuit of Fig. 3 in accordance with one embodiment of the
21 present invention;

22 Fig. 7A is a schematic diagram of an 8-T CAM cell in
23 accordance with one variation of the present invention;

24 Fig. 7B is a schematic diagram of an 8-T CAM cell in
25 accordance with another variation of the present
26 invention;

27 Fig. 8, which consists of Figs. 8A and 8B as
28 illustrated, is a schematic diagram of a 2x2 array of
29 nine-transistor CAM cells in accordance with another
30 embodiment of the present invention;

Fig. 9 is a schematic diagram of the sensor circuit of Fig. 8 in accordance with one embodiment of the present invention;

Fig. 10A is a schematic diagram of an 8-T CAM cell in accordance with one variation of the present invention; and

Fig. 10B is a schematic diagram of an 8-T CAM cell in accordance with another variation of the present invention.

DETAILED DESCRIPTION

Fig. 3, which consists of Figs. 3A and 3B as illustrated, is a schematic diagram of an array of nine-transistor CAM cells 100, 200, 300 and 400. CAM cell 100 includes read/write bit lines 101-102, compare bit lines 103-104, word line 105, p-channel transistors 110-111, n-channel transistors 112-118, and diode element 119. P-channel transistors 110-111 and n-channel transistors 112-115 are connected as a six-transistor SRAM cell. More specifically, transistors 110 and 112 are connected in series between the V_{CC} supply terminal and the ground supply terminal to form a first inverter 121. Similarly, transistors 111 and 113 are connected between the V_{CC} supply terminal and the ground supply terminal to form a second inverter 122. Inverters 121 and 122 are cross-coupled, thereby forming a storage latch that stores a data value D_0 . The output terminal of inverter 121 is labeled node N1, and the output terminal of inverter 122 is labeled node N2.

N-channel transistor 114 is coupled as an access transistor between node N1 and read/write bit line 101. Similarly, n-channel transistor 115 is coupled as an

access transistor between node N2 and read/write bit line 102. Read/write bit lines 101 and 102 are coupled to receive read/write data values D_0 and $D_0\#$, respectively, from column decoder circuitry (not shown). Read/write data value D_0 has a logic high value of V_{CC} and a logic low level of 0 Volts during a write operation. Similarly, read/write data value $D_0\#$ has a logic high value of V_{CC} and a logic low level of $V_{CC}-\Delta V$ during a read operation (where ΔV is about 300 mV). The gates of access transistors 114 and 115 are commonly connected to word line 105. Word line 105 is coupled to receive word line signal WL_0 from row decoder circuitry (not shown). The word line signal WL_0 has a logic high value of V_{CC} and a logic low value of 0 Volts.

Comparison bit lines 103 and 104 are coupled to receive comparison data values CD_0 and $CD_0\#$ from bit line control circuit 120, which is described in more detail below in connection with Fig. 5. Comparison data value CD_0 has a logic high value of 0.6 Volts, a logic low value of 0 Volts, and a pre-charge value of 0.3 Volts. Thus, the voltages used during a comparison operation are much lower than the V_{CC} supply voltage. Moreover, bit line control circuit 120 operates in response to a supply voltage V_{CC1} , which is much less than the V_{CC} supply voltage. In the described embodiment, the V_{CC1} supply voltage is about 0.9 Volts. As a result, the power requirements of CAM cell 100 are much less than a conventional 9-T CAM cell. In addition, the bit lines 103-104 used to perform a comparison are not coupled to the 6-T SRAM cell. As a result, the comparison operation is not burdened by the capacitance introduced by the 6-T SRAM cell. N-channel transistors 116 and 117 are connected in series between

bit lines 103 and 104. Transistors 116 and 117 are commonly connected at node N3. The gates of transistors 116 and 117 are connected to nodes N1 and N2, respectively. Node N3 is coupled to a match sense line 150 through diode element 119 and n-channel transistor 118. Match sense line 150 is coupled to sensor circuit 130.

Diode element 119 can be implemented in various ways, including a conventional p-n junction or a diode-connected transistor. Figs. 4A and 4B are schematic diagrams of diode connected transistors 119A and 119B, respectively, that can be used to implement diode element 119 in accordance with various embodiments of the invention. Thus, diode element 119 is counted as one of the nine transistors of CAM cell 100. As described in more detail below, n-channel transistor 118 is an optional local masking transistor. Because local masking transistor 118 is optional, this transistor is typically not included in determining the transistor count of CAM cell 100. Local masking transistor 118 is coupled to receive a local mask enable signal LM#1. Fig. 4c is a schematic diagram illustrating local masking transistor 118 coupled to diode connected transistor 119A in accordance with another variation.

CAM cell 200 includes read/write bit lines 201-202, comparison bit lines 203-204, word line 105, p-channel transistors 210-211, n-channel transistors 212-218, and diode element 219. The elements of CAM cell 200 are connected in the same manner as the elements of CAM cell 100. CAM cell 200 is connected to word line 105 in the same manner as CAM cell 100. Similarly, CAM cell 200 is connected to match sense line 150 in the same manner as

1 CAM cell 100. Read/write bit lines 201 and 202 of CAM
2 cell 200 are coupled to receive read/write data values D_1
3 and $D_1\#$ from column control circuitry (not shown).
4 Comparison bit lines 203 and 204 of CAM cell 200 are
5 coupled to receive comparison data values CD_1 and $CD_1\#$ from
6 bit line control circuit 220.

7 CAM cell 300 includes read/write bit lines 101-102,
8 comparison bit lines 103-104, word line 106, p-channel
9 transistors 310-311, n-channel transistors 312-318, and
10 diode element 319. Similarly, CAM cell 400 includes
11 read/write bit lines 201-202, comparison bit lines 203-
12 204, word line 106, p-channel transistors 410-411, n-
13 channel transistors 412-418, and diode element 419. The
14 elements of CAM cells 300 and 400 are connected in the
15 same manner as the elements of CAM cell 100. CAM cells
16 300 and 400 are coupled to a second word line 106 in the
17 same manner that CAM cells 100 and 200 are coupled to word
18 line 105. Similarly, CAM cells 300 and 400 are coupled to
19 a second match sense line 151 in the same manner that CAM
20 cells 100 and 200 are coupled to match sense line 150.
21 Match sense line 151 is coupled to a sensor circuit 131,
22 which is identical to sensor circuit 130. Note that CAM
23 cells 100 and 300 share bit lines 101-104. Similarly, CAM
24 cells 200 and 400 share bit lines 201-204.

25 Although the array illustrated in Fig. 3 only has two
26 rows and two columns of CAM cells, it is understood that
27 this array can be expanded to include many more rows and
28 columns of CAM cells. The manner of expansion is obvious
29 in view of the 2x2 array of CAM cells 100, 200, 300 and
30 400 shown in Fig. 3. In a particular example, an array of
31 CAM cells includes eight rows and seventy-two columns of
32 CAM cells.

1 Data values are written to a row of CAM cells (e.g.,
2 CAM cells 100 and 200), as follows. The voltage WL_0 on
3 word line 105 is pulled up to the V_{CC} supply voltage (e.g.,
4 2.5 Volts) by the row decoder circuitry. As a result,
5 access transistors 114-115 and 214-215 are turned on,
6 thereby coupling bit lines 101-102 and 201-202 to the
7 storage latches in CAM cells 100 and 200. The voltage WL_1
8 on the second word line 106 is pulled down to 0 Volts,
9 thereby turning off access transistors 314-315 and 414-415
10 in CAM cells 300 and 400. As a result, bit lines 101-102
11 and 201-202 are isolated from the storage latches in CAM
12 cells 300 and 400.

13 The column decoder circuitry applies write data
14 values D_0 , $D_0\#$, D_1 , and $D_1\#$ to bit lines 101, 102, 201 and
15 202, respectively. These write data values have a logic
16 high value equal to the V_{CC} supply voltage and a logic low
17 value of 0 Volts. In the described example, data values
18 D_0 , $D_0\#$, D_1 , and $D_1\#$ have values of V_{CC} , 0, 0 and V_{CC} ,
19 respectively. The write data values D_0 , $D_0\#$, D_1 , and $D_1\#$
20 are transmitted through turned on access transistors 114-
21 115 and 214-215 to the storage latches in CAM cells 100
22 and 200. The word line signal WL_0 is then de-asserted low,
23 thereby turning off access transistors 114-115 and 214-
24 215, and latching the write data values D_0 , $D_0\#$, D_1 , and $D_1\#$
25 in the storage latches of CAM cells 100 and 200. Write
26 operations are therefore performed in the same manner as
27 in a conventional six-transistor SRAM array. In the
28 present example, nodes N1, N2, N4 and N5 store voltages of
29 V_{CC} , 0 Volts, 0 Volts and V_{CC} , respectively.

30 Data values are read from a row of CAM cells (e.g.,
31 CAM cells 100 and 200), as follows. The column decoder
32 circuitry applies the V_{CC} supply voltage to read/write bit

lines 101, 102, 201 and 202. The voltage WL_0 on word line 105 is pulled up to the V_{CC} supply voltage (e.g., 2.5 Volts) by the row decoder circuitry. As a result, access transistors 114-115 and 214-215 are turned on, thereby coupling bit lines 101-102 and 201-202 to the storage latches in CAM cells 100 and 200. The voltage WL_1 on the second word line 106 is pulled down to 0 Volts, thereby turning off access transistors 314-315 and 414-415 in CAM cells 300 and 400. As a result, bit lines 101-102 and 201-202 are isolated from the storage latches in CAM cells 300 and 400.

In the present example, nodes N2 and N4 are pulled down through transistors 113 and 212, respectively. When access transistors 115 and 214 are turned on, bit lines 102 and 201 are pulled down by transistors 113 and 212, respectively. Nodes N2 and N4 are pulled down to $V_{CC}-\hat{C}V$ at this time, where $\hat{C}V$ is approximately 300 mV. Bit lines 101 and 202 are not pulled down in this manner. Sense amplifiers (not shown) coupled to bit lines 101-102 and 201-202 sense the different voltages on these bit lines to identify the data values stored by CAM cells 100 and 200. Read operations are therefore performed in the same manner as in a conventional six-transistor SRAM array.

During standby conditions, word lines 105 and 106 are maintained at 0 Volts, thereby isolating the CAM cells 100, 200, 300 and 400 from read/write bit lines 101-102 and 201-202. Read/write bit lines 101-102 and 201-202 are held at either V_{CC} or 0 Volts during standby conditions.

A compare operation is performed as follows. During a compare operation, word lines 105 and 106 are maintained at a voltage of 0 Volts, thereby isolating the CAM cells 100, 200, 300 and 400 from bit lines 101-102 and 201-202.

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1 Read/write bit lines 101-102 and 201-202 are held at
2 either V_{CC} or 0 Volts during a compare operation. A
3 compare operation is simultaneously performed within each
4 CAM cell of the array, unless there is global or local
5 masking that inhibits the compare operation within the CAM
6 cell. For purposes of clarity, a compare operation within
7 CAM cell 100 is described in detail. The compare
8 operations performed within CAM cells 200, 300 and 400 are
9 identical to the compare operation performed within CAM
10 cell 100.

11 The compare operation within CAM cell 100 is
12 controlled by bit line control circuit 120 and sensor
13 circuit 130. In general, the data value in the storage
14 latch of CAM cell 100 turns on one and only one of
15 transistors 116 and 117, thereby coupling one of the
16 comparison bit lines 103-104 to node N3. Prior to the
17 comparison operation, node N3 and comparison bit lines
18 103-104 are maintained at 0.3 Volts (assuming there is no
19 global masking enabled by bit line control circuit 120).
20 Local masking transistor 118 is turned on (assuming there
21 is no local masking enabled within CAM cell 100). Sensor
22 circuit 130 maintains match sense line 150 at a voltage of
23 0.6 Volts. A 0.3 Volt forward voltage drop therefore
24 exists across diode-connected transistor 119A.

25 To initiate the comparison operation, bit line
26 control circuit 120 applies comparison data values CD_0 and
27 $CD_0\#$ to comparison bit lines 103 and 104, respectively.
28 The logic high comparison data value has a voltage of 0.6
29 Volts, and the logic low comparison data value has a
30 voltage of 0 Volts. If the comparison data value matches
31 the data value stored in CAM cell 100, then a voltage of
32 0.6 Volts is applied to node N3. Under these conditions,

1 the voltage on match sense line 150 remains at 0.6 Volts.
2 If the comparison data value does not match the data value
3 stored in CAM cell 100, then a voltage of 0 Volts is
4 applied to node N3. Under these conditions, the voltage
5 on match sense line 150 is pulled down to 0.3 Volts.
6 Sensor circuit 130 senses the voltage on match sense line
7 150, and indicates a match condition if match sense line
8 150 is maintained at 0.6 Volts, and indicates a no-match
9 condition if match sense line 150 is pulled down to 0.3
10 Volts. Because the full signal swing on match sense line
11 150 is equal to 0.3 Volts, and because the comparison bit
12 lines are operated at voltages much less than the V_{CC}
13 supply voltage, the power requirements of a compare
14 operation are advantageously very low in CAM cell 100.

15 Local masking signal $LM\#_1$ is an active low signal. If
16 the local masking signal $LM\#_1$ has a logic low value, local
17 masking transistor 118 is turned off, thereby isolating
18 node N3 from match sense line 150. Under these
19 conditions, match sense line is maintained at 0.6 Volts,
20 regardless of the results of the comparison within CAM
21 cell 100. CAM cell 100 therefore performs as if a match
22 condition exists, regardless of the results of the
23 comparison within CAM cell 100. In this manner, local
24 masking transistor 118 enables CAM cell 100 to be
25 effectively masked from the comparison operation.
26 Although Fig. 3 indicates that local masking transistor
27 118 is coupled between diode 119 and match line 150, it is
28 understood that local masking transistor 118 can be
29 coupled between diode 119 and node N3 to achieve similar
30 results. Fig. 4C is a schematic diagram illustrating
31 another possible arrangement of diode-connected transistor

1 119A and local masking transistor 118. Other variations
2 are apparent to those of ordinary skill in the art.

3 Bit line control circuit 120 and sensor circuit 130
4 will now be described in more detail. Fig. 5 is a
5 schematic diagram of sensor circuit 130. Sensor circuit
6 130 includes inverters 501-502, current sources 503-504,
7 NAND gate 505 and n-channel transistors 511-515, which are
8 connected as illustrated. During a pre-charge period
9 before the compare operation is performed, the CLK1 and
10 CLK2 signals have logic low values. The logic low CLK2
11 signal causes transistor 511 to turn on, thereby coupling
12 the V_{CC1} supply voltage to the drain of transistor 513. In
13 the described example, the V_{CC1} supply voltage is equal to
14 approximately three times the threshold voltage of an n-
15 channel transistor, or about 0.9 Volts. The logic low
16 CLK1 signal causes NAND gate 505 to provide a logic high
17 output signal (e.g., 2.5 Volts) to the gate of transistor
18 512, thereby turning on this transistor. As a result,
19 transistor 512 also helps to pull up the voltage on the
20 drain of transistor 513 to the V_{CC1} supply voltage.

21 Under these conditions, transistors 514 and 515 are
22 turned on by current source 504. Each of transistors 514
23 and 515 has a threshold voltage of 0.3 Volts. As a
24 result, the voltage on match sense line 150 is held at 0.6
25 Volts. At this time, the voltage on node N3 is equal to
26 0.3 Volts, or one threshold voltage below the voltage on
27 match sense line 150.

28 The compare operation begins when the CLK2 signal
29 goes high. The CLK2 signal transitions to a logic high
30 state shortly before the CLK1 signal transitions to a
31 logic high state. As a result, the output signal provided
32 by NAND gate 505 remains high for a short time after the

1 CLK2 signal goes high. This ensures that transistor 512
2 remains on while the CLK2 signal goes high, thereby
3 preventing noise conditions from pulling down the voltage
4 on match sense line 150. The CLK1 signal then transitions
5 to a logic high value, such that the output voltage
6 provided by NAND gate 505 is determined by the state of
7 the voltage on match sense line 150. At this time, node
8 N3 is either pulled up to 0.3 Volts (if a match condition
9 exists) or pulled down to 0 Volts (if a no-match condition
10 exists).

11 As described in more detail below, during a match
12 condition node N3 will be coupled to a comparison bit line
13 having a voltage of 0.6 Volts through either transistor
14 116 or transistor 117. Under these conditions, no current
15 flows through transistor 513. As a result, the gate of
16 transistor 513 is maintained at about 0.6 Volts. This 0.6
17 Volt signal represents a logic low input signal to NAND
18 gate 505. As a result, NAND gate 505 provides a logic
19 high output signal to transistor 512. Transistor 512
20 therefore remains on (even though there is no current
21 flow). If the signal on match sense line 150 is pulled
22 low by noise, then current source 503 will pull the
23 voltage on match sense line 150 back up to 0.6 Volts
24 through turned on transistor 512.

25 The logic high output of NAND gate 505 is also
26 provided to inverter 502. In response, inverter 502
27 provides a logic low output signal having a voltage equal
28 to the ground supply voltage (e.g., 0 Volts). This output
29 signal is used to indicate a match condition to an encoder
30 circuit (not shown).

31 As described in more detail below, during a no-match
32 condition node N3 will be coupled to a comparison bit line

1 having a voltage of 0 Volts through either transistor 116
2 or transistor 117. As a result, node N3 is pulled down to
3 0 Volts. Under these conditions, current will flow
4 through transistor 513. This current is greater than the
5 current provided by current source 503. As a result, the
6 voltage of match sense line 150 is pulled down to 0.3
7 Volts (i.e., one threshold voltage greater than the
8 voltage on node N3). The 0.3 Volt signal on match sense
9 line 150 causes the voltage on the gate of transistor 513
10 to be pulled up to the V_{CC} supply voltage (e.g., 2.5 Volts)
11 by current source 504. This V_{CC} supply voltage represents
12 a logic high input signal to NAND gate 505. Consequently,
13 NAND gate 505 provides a logic low output signal to the
14 gate of transistor 512. As a result, transistor 512 is
15 turned off, thereby preventing DC current flow through
16 transistor 513.

17 The logic low output of NAND gate 505 is also
18 provided to inverter 502. In response, inverter 502
19 provides a logic high output signal having a voltage equal
20 to the V_{CC} supply voltage (e.g., 2.5 Volts). This output
21 signal is used to indicate a no-match condition to an
22 encoder circuit (not shown).

23 Although the operation of sensor circuit 130 has been
24 described in connection with a single CAM cell 100, it is
25 understood that a match condition must exist in all of the
26 CAM cells coupled to match sense line 150 in order for
27 sensor circuit 130 to provide a logic high output signal
28 to the encoder. Conversely, if a no-match condition
29 exists in any one of the CAM cells coupled to match sense
30 line 150, then sensor circuit 130 will provide a logic low
31 output signal to the encoder.

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Fig. 6 is a schematic diagram of bit line control circuit 120. Bit line control circuit 121 is identical to bit line control circuit 120. Bit line control circuit 120 includes inverters 601-609, NAND gates 611-612, n-channel transistors 621-630 and current source 631, which are connected as illustrated. In general, bit line control circuit 120 provides voltages on comparison bit lines 103-104 in response to a comparison data input value D_{IN} , the clock signal CLK2, and a global masking signal GM#.

Bit line control circuit 120 operates as follows. Transistors 628-630 and current source 631 are connected to form a regulated voltage source 640. Current source 631, which operates in response to the V_{CC} supply voltage, turns on transistors 629 and 630. Each of transistors 629 and 630 has a threshold voltage of 0.3 Volts. As a result, the voltage on voltage supply line 650 is held at 0.6 Volts. Transistor 628, which is coupled to the V_{CC1} voltage supply (0.9 Volts), is turned on to help pull up voltage supply line 650 to 0.6 Volts. In the described embodiment, the voltage on voltage supply line 650 is selected to be equal to two times the threshold voltage of an n-channel transistor (i.e., 0.3 Volts).

Global masking signal GM# is an active low signal. When the global masking signal GM# has a logic low value, inverters 602-604 provide a logic high signal to transistors 621 and 622, thereby turning on these transistors. The logic low GM# signal causes transistors 623-626 to be turned off. Transistor 627 is either turned off or turned on, depending on the state of the CLK2 signal. Under these conditions, both of comparison bit lines 103 and 104 are connected to receive a voltage of

20

0.6 Volts from voltage supply line 650. If both of comparison bit lines 103 have a voltage of 0.6 Volts, then all of the CAM cells in the column served by bit line control circuit 120 will indicate a match condition during a compare operation. As a result, the entire column is effectively masked during such a compare operation.

When the global masking signal GM# is de-asserted high, transistors 621 and 622 are turned off. During this time, the CLK2 signal can have a logic low or logic high value. A pre-charge operation is performed if the CLK2 signal has a logic low value, and a compare operation is performed if the CLK2 signal has a logic high value. If the CLK2 signal has a logic low value, transistor 627 is turned on, thereby connecting comparison bit lines 103 and 104. The logic low CLK2 signal further causes transistors 623-626 to turn off, thereby isolating comparison bit lines 103 and 104 from voltage supply line 650 and the ground voltage supply. As a result, the voltages on both bit lines 103 and 104 are equalized at 0.3 Volts by sensor circuit 130 during the pre-charge operation. Note that the comparison data input value D_{IN} does not have any effect on transistors 623-627 when the CLK2 signal has a logic low value.

A compare operation occurs when the CLK2 signal transitions to a logic high value (and the GM# signal is de-asserted high). Under these conditions, transistors 621-622 and 627 are turned off. Comparison data input value D_{IN} is asserted at this time. A comparison data input value D_{IN} having a logic high state will turn on transistors 623 and 624 (and turn off transistors 625 and 626), thereby applying 0.6 Volts to comparison bit line 103 and 0 Volts to comparison bit line 104. Conversely, a

1 comparison data input value D_{IN} having a logic low state
2 will turn on transistors 625 and 626 (and turn off
3 transistors 623 and 624), thereby applying 0.6 Volts to
4 comparison bit line 104 and 0 Volts to comparison bit line
5 103.

6 Although the present invention has been described in
7 connection with particular embodiments, other embodiments
8 are possible and are considered to be within the scope of
9 the present invention. Fig. 7A is a schematic diagram of
10 an 8-T CAM cell 700A in accordance with one variation of
11 the present invention. Similar elements in CAM cell 100
12 (Fig. 3) and CAM cell 700A are labeled with similar
13 reference numbers. CAM cell 700A includes the same
14 elements as CAM cell 100, with the exception of access
15 transistor 115 and bit line 102, which are not present in
16 CAM cell 700A. CAM cell 700A is written and read through
17 bit line 101 and access transistor 114. The compare
18 operation of CAM cell 700A is identical to the compare
19 operation of CAM cell 100. CAM cell 700A advantageously
20 uses one less transistor and one less bit line than CAM
21 cell 100. Note that the above-described variations of CAM
22 cell 100 can also be applied to CAM cell 700A.

23 Fig. 7B is a schematic diagram of an 8-T CAM cell
24 700B in accordance with another variation of the present
25 invention. Similar elements in CAM cell 100 (Fig. 3) and
26 CAM cell 700B are labeled with similar reference numbers.
27 CAM cell 700B includes the same elements as CAM cell 100,
28 with the exception of access transistor 115 and bit lines
29 102 and 103, which are not present in CAM cell 700B. CAM
30 cell 700B is written and read through bit line 101 and
31 access transistor 114. The compare operation of CAM cell
32 700B is similar to the compare operation of CAM cell 100.

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1 However, the comparison data value CD_0 is provided on bit
2 line 101 in this variation. Selection circuitry (not
3 shown) is provided to selectively couple bit line 101 to
4 the above-described column select circuitry (not shown)
5 during a read or a write operation, or to the bit line
6 control circuit 120 during a compare operation. CAM cell
7 700B advantageously uses one fewer transistor and two
8 fewer bit lines than CAM cell 100. Note that the above-
9 described variations of CAM cell 100 can also be applied
10 to CAM cell 700B.

11 Fig. 8, which consists of Figs. 8A and 8B as
12 illustrated, is a schematic diagram of an array of nine-
13 transistor CAM cells 1000, 2000, 3000 and 4000. Because
14 CAM cells 1000, 2000, 3000 and 4000 are similar to CAM
15 cells 100, 200, 300 and 400 (Fig. 3), similar elements in
16 Figs 3 and 8 are labeled with similar reference numbers.
17 CAM cell 1000 replaces diode element 119, local masking
18 transistor 118 and match sense line 150 of CAM cell 100
19 with match transistor 1190, local masking transistor 1180
20 and match sense lines 1500 and 1510. Transistors 1180 and
21 1190 are connected in series between match sense lines
22 1500 and 1510. The gate of match transistor 1190 is
23 coupled to node N3. Both of match sense lines 1500 and
24 1510 are connected to sensor circuit 1300.

25 CAM cells 2000, 3000 and 4000 include similar match
26 transistors 2190, 3190 and 4190 and similar local masking
27 transistors 2180, 3180 and 4180. CAM cells 3000 and 4000
28 share match sense lines 1520 and 1530, which in turn, are
29 connected to sensor circuit 1310.

30 Bit line control circuits 1200 and 2200 are connected
31 to comparison bit lines 103-104 and 203-204, respectively.

23

Although the array illustrated in Fig. 8 only has two rows and two columns of CAM cells, it is understood that this array can be expanded to include many more rows and columns of CAM cells. The manner of expansion is obvious in view of the 2x2 array of CAM cells 1000, 2000, 3000 and 4000 shown in Fig. 8.

Because CAM cells 1000, 2000, 3000 and 4000 are identical, only CAM cell 1000 is described in detail. Similarly, because sensor circuits 1300 and 1310 are identical, only sensor circuit 1300 is described in detail.

CAM cell 1000 reverses the polarity of the comparison data values CD_0 and $CD_0\#$ provided by bit line control circuit 120, such that comparison data value $CD_0\#$ is applied to comparison bit line 103, and comparison data value CD_0 is applied to comparison bit line 104. In addition, voltage supply line 650 is directly connected to the V_{CC1} supply voltage of 0.9 Volts ($3V_T$) instead of to regulated voltage source 640. Otherwise, the bit line control circuit 1200 is identical to bit line control circuit 120 (Fig. 6).

Read, write and standby operations are performed within CAM cell 1000 in the same manner described above in connection with CAM cell 100.

A compare operation is performed within CAM cell 1000 as follows. During a compare operation, word lines 105 and 106 are maintained at a voltage of 0 Volts, thereby isolating the CAM cells 1000, 2000, 3000 and 4000 from bit lines 101-102 and 201-202. Read/write bit lines 101-102 and 201-202 are held at either V_{CC} or 0 Volts during a compare operation. A compare operation is simultaneously performed within each CAM cell of the array, unless there

1 is global or local masking that inhibits the compare
2 operation within the CAM cell. For purposes of clarity, a
3 compare operation within CAM cell 1000 is described in
4 detail. The compare operations performed within CAM cells
5 2000, 3000 and 4000 are identical to the compare operation
6 performed within CAM cell 1000.

7 The compare operation within CAM cell 1000 is
8 controlled by bit line control circuit 1200 and sensor
9 circuit 1300. In general, the data value in the storage
10 latch of CAM cell 1000 turns on one and only one of
11 transistors 116 and 117, thereby coupling one of the
12 comparison bit lines 103-104 to node N3. Prior to the
13 comparison operation, node N3 and comparison bit lines
14 103-104 are maintained at 0.3 Volts (assuming there is no
15 global masking enabled by bit line control circuit 1200).
16 Local masking transistor 1180 is turned on (assuming there
17 is no local masking enabled within CAM cell 1000). Sensor
18 circuit 1300 maintains match sense lines 1500 and 1510 at
19 0.3 Volts.

20 To initiate the comparison operation, bit line
21 control circuit 1200 applies comparison data values CD_0 and
22 $CD_0\#$ to comparison bit lines 104 and 103, respectively.
23 The logic high comparison data value has a voltage of 0.9
24 Volts (i.e., V_{CC1} or $3V_T$), and the logic low comparison data
25 value has a voltage of 0 Volts. If the comparison data
26 value matches the data value stored in CAM cell 1000, then
27 a voltage of 0 Volts is applied to node N3. Under these
28 conditions, match transistor 1190 is turned off, thereby
29 allowing the voltage on match sense line 1500 to remain at
30 0.3 Volts. If the comparison data value does not match
31 the data value stored in CAM cell 1000, then a voltage of
32 0.9 Volts is applied to node N3. Under these conditions,

1 match transistor 1190 turns on, thereby pulling down the
2 voltage on match sense line 1500 down to 0 Volts. Sensor
3 circuit 1300 senses the voltage on match sense line 1500,
4 and indicates a no-match condition if match sense line
5 1500 is pulled down to 0 Volts, and indicates a match
6 condition if match sense line 1500 remains at 0.3 Volts.
7 Because the full signal swing on match sense line 1500 is
8 equal to 0.3 Volts, and because the bit line control
9 circuit 1200 is powered by the V_{CC1} supply voltage, the
10 power requirements of a compare operation are
11 advantageously very low in CAM cell 1000.

12 Local masking signal $LM\#_1$ is an active low signal. If
13 the local masking signal $LM\#_1$ has a logic low value, local
14 masking transistor 1180 is turned off, thereby isolating
15 match sense lines 1500 and 1510. Under these conditions,
16 match sense line is maintained at 0.3 Volts, regardless of
17 the results of the comparison within CAM cell 1000. CAM
18 cell 1000 therefore performs as if a match condition
19 exists, regardless of the results of the comparison within
20 CAM cell 1000. In this manner, local masking transistor
21 1180 enables CAM cell 1000 to be effectively masked from
22 the comparison operation. Although Fig. 8 indicates that
23 local masking transistor 1180 is coupled between match
24 transistor 1190 and match sense line 1510, it is
25 understood that local masking transistor 1180 can be
26 coupled between match transistor 1190 and match sense line
27 1500 to achieve similar results.

28 Fig. 9 is a schematic diagram of sensor circuit 1300.
29 Because sensor circuit 1300 is similar to sensor circuit
30 130 (Fig. 5), similar elements in Figs. 5 and 9 are
31 labeled with similar reference numbers. Sensor circuit
32 1300 eliminates transistor 515 of sensor circuit 130, such

1 that the source of transistor 514 is connected to ground.
2 Sensor circuit 1300 further includes n-channel transistor
3 516, which is connected in series across match lines 1500
4 and 1510. The gate of transistor 516 is connected to the
5 output terminal of inverter 501. Sensor circuit 1300 also
6 includes n-channel transistor 517, which is connected
7 between match sense line 1510 and the ground supply
8 terminal. The gate of transistor 517 is coupled to
9 receive the CLK2 signal.

10 During a pre-charge period before the compare
11 operation is performed, the CLK1 and CLK2 signals have
12 logic low values. The logic low CLK2 signal causes
13 transistor 511 to turn on, thereby coupling the V_{CC1} supply
14 voltage to the drain of transistor 513. In the described
15 example, the V_{CC1} supply voltage is equal to approximately
16 three times the threshold voltage of an n-channel
17 transistor, or about 0.9 Volts. The logic low CLK1 signal
18 causes NAND gate 505 to provide a logic high output signal
19 (e.g., 2.5 Volts) to the gate of transistor 512, thereby
20 turning on this transistor. As a result, transistor 512
21 also helps to pull up the voltage on the drain of
22 transistor 513 to the V_{CC1} supply voltage.

23 Under these conditions, transistor 514 is turned on
24 by current source 504. Transistor 514 has a threshold
25 voltage of 0.3 Volts. As a result, the voltage on match
26 sense line 1500 is held at 0.3 Volts. The logic low CLK2
27 signal causes transistor 516 to turn on, thereby coupling
28 match sense lines 1500 and 1510. Consequently, match
29 sense line 1510 is also held at 0.3 Volts.

30 The compare operation begins when the CLK2 signal
31 goes high. The logic high CLK2 signal causes transistors
32 511 and 516 to be turned off. The CLK2 signal transitions

to a logic high state shortly before the CLK1 signal transitions to a logic high state. As a result, the output signal provided by NAND gate 505 remains high for a short time after the CLK2 signal goes high. This ensures that transistor 512 remains on while the CLK2 signal goes high, thereby preventing noise conditions from pulling down the voltage on match sense line 1500. The CLK1 signal then transitions to a logic high value, such that the output voltage provided by NAND gate 505 is determined by the state of the voltage on match sense line 1500. At this time, node N3 is either pulled up to 0.9 Volts (if a no-match condition exists) or pulled down to 0 Volts (if a match condition exists).

As previously described, during a no-match condition node N3 will be coupled to a comparison bit line having a voltage of 0.9 Volts through either transistor 116 or transistor 117. Under these conditions, match transistor 1190 turns on, and current flows through transistor 513. This current is greater than the current provided by current source 503. As a result, the voltage of match sense line 1500 is pulled down to 0 Volts. The 0 Volt signal on match sense line 1500 causes the voltage on the gate of transistor 513 to be pulled up to the V_{CC} supply voltage (e.g., 2.5 Volts) by current source 504. This V_{CC} supply voltage represents a logic high input signal to NAND gate 505. Consequently, NAND gate 505 provides a logic low output signal to the gate of transistor 512. As a result, transistor 512 is turned off, thereby preventing DC current flow through transistor 513.

The logic low output of NAND gate 505 is also provided to inverter 502. In response, inverter 502 provides a logic high output signal having a voltage equal

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1 to the V_{cc} supply voltage (e.g., 2.5 Volts). This output
2 signal is used to indicate a no-match condition to an
3 encoder circuit (not shown).

4 As described above, during a match condition node N3
5 will be coupled to a comparison bit line having a voltage
6 of 0 Volts through either transistor 116 or transistor
7 117. As a result, no current flows through transistor
8 513. Consequently, the gate of transistor 513 is
9 maintained at about 0.3 Volts. This 0.3 Volt signal
10 represents a logic low input signal to NAND gate 505. As
11 a result, NAND gate 505 provides a logic high output
12 signal to transistor 512. Transistor 512 therefore
13 remains on (even though there is no current flow). If the
14 signal on match sense line 1500 is pulled low by noise,
15 then current source 503 will pull the voltage on match
16 sense line 1500 back up to 0.3 Volts through turned on
17 transistor 512.

18 The logic high output of NAND gate 505 is also
19 provided to inverter 502. In response, inverter 502
20 provides a logic low output signal having a voltage equal
21 to 0 Volts. This output signal is used to indicate a
22 match condition to an encoder circuit (not shown).

23 Although the operation of sensor circuit 1300 has
24 been described in connection with a single CAM cell 1000,
25 it is understood that a match condition must exist in all
26 of the CAM cells coupled to match sense line 1500 in order
27 for sensor circuit 1300 to provide a logic low output
28 signal to the encoder. Conversely, if a no-match
29 condition exists in any one of the CAM cells coupled to
30 match sense line 1500, then sensor circuit 1300 will
31 provide a logic high output signal to the encoder.

29

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1 Although the present invention has been described in
2 connection with particular embodiments, other embodiments
3 are possible and are considered to be within the scope of
4 the present invention. Fig. 10A is a schematic diagram of
5 an 8-T CAM cell 800A in accordance with one variation of
6 the present invention. Similar elements in CAM cell 1000
7 (Fig. 8) and CAM cell 800A are labeled with similar
8 reference numbers. CAM cell 800A includes the same
9 elements as CAM cell 1000, with the exception of access
10 transistor 115 and bit line 102, which are not present in
11 CAM cell 800A. CAM cell 800A is written and read through
12 bit line 101 and access transistor 114. The compare
13 operation of CAM cell 800A is identical to the compare
14 operation of CAM cell 1000. CAM cell 800A advantageously
15 uses one less transistor and one less bit line than CAM
16 cell 1000. Note that the above-described variations of
17 CAM cell 1000 can also be applied to CAM cell 800A.

18 Fig. 10B is a schematic diagram of an 8-T CAM cell
19 800B in accordance with another variation of the present
20 invention. Similar elements in CAM cell 1000 (Fig. 8) and
21 CAM cell 800B are labeled with similar reference numbers.
22 CAM cell 800B includes the same elements as CAM cell 1000,
23 with the exception of access transistor 115 and bit lines
24 102 and 103, which are not present in CAM cell 800B. CAM
25 cell 800B is written and read through bit line 101 and
26 access transistor 114. The compare operation of CAM cell
27 800B is similar to the compare operation of CAM cell 1000.
28 However, the comparison data value $CD_0\#$ is provided on bit
29 line 101 in this variation. Selection circuitry (not
30 shown) is provided to selectively couple bit line 101 to
31 the above-described column select circuitry (not shown)
32 during a read or a write operation, or to the bit line

1 control circuit 120 during a compare operation. CAM cell
2 800B advantageously uses one fewer transistor and two
3 fewer bit lines than CAM cell 1000. Note that the above-
4 described variations of CAM cell 1000 can also be applied
5 to CAM cell 800B.

6 Although the present invention has been described in
7 connection with several embodiments, it is understood that
8 this invention is not limited to the embodiments
9 disclosed, but is capable of various modifications which
10 would be apparent to one of ordinary skill in the art.
11 Thus, the invention is limited only by the following
12 claims.

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